09/818089

Copy 1 of 2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Jim Stockdale

Attorney Docket No.: IGT1P074X1/P-288 CIP

Patent: 6,875,109

Issued: April 5, 2005

Title: MASS STORAGE DATA PROTECTION SYSTEM FOR A GAMING MACHINE

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on May 3, 2005 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: Tomika Thomas

Tomika D. Thomas

REQUEST FOR CERTIFICATE OF CORRECTION OF OFFICE MISTAKE (35 U.S.C. §254, 37 CFR §1.322)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attn: Certificate of Correction

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing. The errors together with the exact page and line number where the errors are shown correctly in the application file are as follows:

CLAIMS:

1. In line 19 of claim 6 (column 6, line 64) change "stains" to --status--. This appears correctly in the Amendment A filed August 27, 2004, on page 4, line 7.

2. In line 21 of claim 6 (column 6, line 66) change "resister" to --register--. This appears correctly in Amendment A filed August 27, 2004, on page 4, line 8.

3. In line 21 of claim 7 (column 7, line 28) change "resister" to --register--. This appears correctly in Amendment A filed August 27, 2004, on page 5, line 10.

4. In line 3 of claim 11 (column 7, line 47) change "any" to --array--. This appears correctly in Amendment A, filed August 27, 2004, on page 6, line 6.

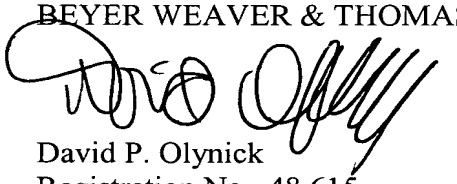
6. In line 23 of claim 12 (column 8, line 20) change "resister" to --register--. This appears correctly in Amendment A, filed August 27, 2004, on page 7, line 2.

7. In line 6 of claim 13 (column 8, line 38) change "close" to --closed--. This appears correctly in Amendment A, filed August 27, 2004, on page 7, line 22.

8. In line 2 of claim 14 (column 8, line 40) change "farther" to --further--. This appears correctly in the patent application as filed on page 7, line 1.

It is noted that the above-identified errors were printing errors that apparently occurred during the printing process. Enclosed please find a copy of Amendment A, submitted in support of our claim. Accordingly, it is believed that no fees are due in connection with the filing of this Request for Certificate of Correction. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. IGT1P074X1).

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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(Also Form PT-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,875,109

DATED : April 5, 2005

INVENTOR(S) : Jim Stockdale

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Claims

In line 19 of claim 6 (column 6, line 64) change "stains" to --status--
In line 21 of claim 6 (column 6, line 66) change "resister" to --register--
In line 21 of claim 7 (column 7, line 28) change "resister" to --register--
In line 3 of claim 11 (column 7, line 47) change "any" to --array--
In line 23 of claim 12 (column 8, line 20) change "resister" to --register--
In line 6 of claim 13 (column 8, line 38) change "close" to --closed--
In line 2 of claim 14 (column 8, line 40) change "farther" to --further--

MAILING ADDRESS OF SENDER:

PATENT NO. 6,875,109

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Stockdale

Application No.: 09/818,089

Filed: March 26, 2001

Title: Mass Storage Protection System for a Gaming Machine

Attorney Docket No.: IGT1P074X1

Examiner: Julie K. Brocketti

Group: 3713

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via facsimile to the U.S. Patent and Trademark Office, Attention: Examiner J. Brocketti at facsimile telephone number (703) 872-9306 on August 27, 2004.

Signed: Tomika Thomas

Tomika Thomas

AMENDMENT A

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Office Action is being re-submitted in compliance with a Notice of Non-Compliant Amendment (37 CFR 1.121). A proper status identifier has been provided for claim one, please amend the above-identified patent application as follows:

Amendments to the Claims are reflected in the listing of claims, which begins on page 2 of this paper.

Remarks/Arguments begin on page 8 of this paper.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A mass storage data protection system for use with a mass storage device in a gaming machine, the mass storage data protection system comprising:

a mass storage device command latch for storing commands from a disk controller;

a timing circuit for timing signals between the mass storage device command latch and the mass storage device;

a comparator between the mass storage device command latch and the timing ~~means~~ circuit; and

a comparator command register in communication with the comparator, the comparator command register including ATA write commands wherein the comparator issues a fault when the mass storage device command latch stores a command matching an ATA command from the comparator command register ~~that generate a fault within the mass storage data protection system; wherein when the comparator receives a command from the mass storage device command latch corresponding to a command within the comparator command register, a fault is generated within the mass storage command latch~~.

2. (Currently Amended) A mass storage data protection system in accordance with claim 1 further comprising a control and status register in communication with the comparator command register and the comparator wherein the control and status register is configured to receive information from the comparator and to send information to the comparator command register and is operable to receive information from a jumper for enabling writing to the mass storage device~~, the control and status register being~~

~~configured to at least partially control functioning of the mass storage data protection system~~.

3. (Original) A mass storage data protection system in accordance with claim 1 wherein the timing circuit comprises a synchronizer and a reset generator.

4. (Original) A mass storage data protection system in accordance with claim 1 wherein the mass storage device consists of an intelligent drive electronics hard disk drive and the mass storage device command latch consists of an intelligent drive electronics command latch.

5. (Original) A mass storage data protection system in accordance with claim 1 where in the comparator command register comprises a fixed command array and a user command array.

6. (Currently Amended) A mass storage data protection system for use with an intelligent drive electronics mass storage device in a gaming machine, the mass storage data protection system comprising:

an intelligent drive electronics mass storage device command latch for storing commands from a disk controller;

a timing circuit for timing signals between the intelligent drive electronics command latch and the intelligent drive electronics mass storage device, the timing circuit comprising a synchronizer and a reset generator;

a comparator comprising a fixed command array and a user command array, the comparator being located between the intelligent drive electronics command latch and the timing circuit ;

a comparator command register in communication with the comparator, the comparator command register including ATA write commands ~~that generate a fault within the mass storage data protection system~~; and

a control and status register in communication with the comparator command register and the comparator, wherein the control and status register is configured to receive information from the comparator and to send information to the comparator command register and is operable to receive information from a jumper for enabling writing to the mass storage device and ~~the control and status register being configured to at least partially control functioning of the mass storage data protection system~~; wherein the comparator issues a fault when the intelligent drive electronics mass storage device command latch stores a command matching an ATA command from the comparator command register ~~wherein when the comparator receives a command from the intelligent drive electronics command latch corresponding to a command within the comparator command register, a fault is generated within the intelligent drive electronics command latch~~.

7. (Currently Amended) A gaming machine comprising:

a housing; at least one user input coupled to the housing;

a display coupled to the housing;

and a control system, the control system comprising:

a mass storage device; and

a mass storage data protection system, the mass storage data protection system comprising:

a mass storage device command latch for storing commands from a disk controller;

a timing circuit for timing signals between the mass storage device command latch and the mass storage device;

a comparator between the mass storage device command latch and the timing circuit; and

a comparator command register in communication with the comparator, the comparator command register including ATA write commands wherein the comparator issues a fault when the mass storage device command latch stores a command matching an ATA command from the comparator command register ~~that generate a fault within the mass storage data protection system; wherein when the comparator receives a command from the mass storage device command latch corresponding to a command within the comparator command register, a fault is generated within the mass storage command latch~~.

8. (Currently Amended) A gaming machine in accordance with claim 7 further comprising a control and status register in communication with the comparator command register and the comparator, wherein the control and status register is configured to receive information from the comparator and to send information to the comparator command register and is operable to receive information from a jumper for enabling writing to the mass storage device ~~the control and status register being configured to at least partially control functioning of the mass storage data protection system~~.

9. (Original) A gaming in accordance with claim 7 wherein the timing circuit comprises a synchronizer and a reset generator.

10. (Original) A gaming machine in accordance with claim 7 wherein the mass storage device consists of an intelligent drive electronics hard disk drive and the mass storage device command latch consists of an intelligent drive electronics command latch.

11. (Original) A gaming machine in accordance with claim 7 wherein the comparator command register comprises a fixed command array and a user command array.

12. (Currently Amended) A gaming machine comprising:

a housing; at least one user input coupled to the housing;

a display coupled to the housing; and

a control system, the control system comprising:

an intelligent drive electronics mass storage device; and

a mass storage data protection system, the mass data protection system comprising:

an intelligent drive electronics mass storage device command latch for storing commands from a disk controller;

a timing circuit for timing signals between the intelligent drive electronics command latch and the intelligent drive electronics mass storage device, the timing circuit comprising a synchronizer and a reset generator;

a comparator comprising a fixed command array and a user command array, the comparator being located between the intelligent drive electronics command latch and the timing circuit wherein the comparator issues a fault when the intelligent drive electronics mass

storage device command latch stores a command matching an ATA command from a comparator command register;

~~a~~ the comparator command register in communication with the comparator, the comparator command register including ATA write commands ~~that generate a fault within the mass storage data protection system~~; and

a control and status register in communication with the comparator command register and the comparator, the control and status register wherein the control and status register is configured to receive information from the comparator and to send information to the comparator command register and is operable to receive information from a jumper or a write enable switch for enabling writing to the mass storage device ~~being configured to at least partially control functioning of the mass storage data protection system; wherein when the comparator receives a command from the intelligent drive electronics command latch corresponding to a command within the comparator command register, a fault is generated within the intelligent drive electronics command latch~~.

13. (Currently Amended) A gaming machine in accordance with claim ~~7~~ 12 wherein the control system further comprises: ~~a~~ the write enable switch in communication with the comparator, the write enable switch being configured to suppress generation of a fault within the mass storage command latch when the write enable switch is closed.

14. (Original) A gaming machine in accordance with claim 13, further comprising: a microprocessor in communication with the mass storage device and the mass storage data

protection system; and gaming machine operating software running on the microprocessor, the gaming machine operating software having at least a gaming mode and a maintenance mode, wherein the gaming machine operating software is configured to suspend gaming operation when the write enable switch is closed and the gaming machine operating software is in a mode other than the maintenance mode.

REMARKS

Claims 1-14 currently remain in the application. Claims 1, 2, 6-8, 12 and 13 have been amended.

Double Patenting

Claims 1-12 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-12 of U.S. patent No. 6, 488, 581. A terminal disclaimer is included with this amendment and the rejection is believed overcome thereby.

Rejections under 35 U.S.C. § 112

Claims 2, 6, 8 and 12-14 are rejected under 35 U.S.C. § 112, second paragraph. Claims 2, 6, 8 and 12 have been amended for the purposes of clarification to remove the "at least partially" term objected to by the Examiner and the rejection is believed overcome thereby.

Claim 13 has been amended to depend from claim 12 and the rejection to claims 13 and 14 are believed overcome thereby.

Rejections under 35 U.S.C. § 103

The Examiner rejected claims 1, 3 and 5 under U.S.C. 103 (a) as being unpatentable over Sugai (5,564,036) in view of Ciciora (US patent No. 4,091, 418). The rejection is respectfully traversed.

The claims describe, as recited in claim 1, for instance, a mass storage device command latch for storing commands from a disk controller; a timing circuit for timing signals between the mass storage device command latch and the mass storage device; a comparator between the mass storage device command latch and the timing circuit; and a comparator command register in communication with the comparator, the comparator command register including ATA write commands where the comparator issues a fault when the mass storage device command latch stores a command matching an ATA command from the comparator command register.

Prior IDE systems known to the Applicant were designed to allow read and write operations to a mass storage device. The IDE standard provides as much; it defines a set of read and write commands. There was no incentive to prevent writing to an IDE mass storage device. It is only in the context of a gaming machine where one confronts a need to disable the write capabilities of the IDE protocol in a manner that a fault is issued when a write is detected. The claims recite a system that protects a mass storage device or an IDE mass storage device in a gaming machine from write operations. To this effect, the claims require that the comparator command register include ATA write commands that can be compared against commands from a disk controller. The comparator issues a fault when the mass storage device command latch stores a command matching an ATA command from the comparator command register. Typically, the fault will cause the gaming machine to cease gaming operations which is a feature unique to gaming.

Sugai, Cols. 1 and 2, describes detecting addresses in RAM and writing those addresses into latch memory by the CPU. Because Sugai does not protect mass storage devices but RAM from write operations, does not detect commands, only addresses, where the addresses are provided by the CPU not the disk controller, it is respectfully submitted that pending claims are patentable over the Sugai patent. Ciciora does not overcome these deficiencies. All claims require a system that can detect ATA write commands where the comparator issues a fault when the mass storage device command latch stores a command matching an ATA command from the comparator command register where the mass storage device command latch stores commands from a disk controller. These limitations are not taught or suggested by Sugai or Ciciora. Therefore, for at least these reasons, Sugai and Ciciora alone or in combination can't be said to render obvious the present invention and the rejection of claims 1, 3 and 5 is believed overcome thereby.

The Examiner rejected claims 2, 4 and 6 under U.S.C. 103 (a) as being unpatentable over Sugai (5,564,036) in view of Ciciora (4,091, 418) and in further view of Browne (6,272,533). The rejection is respectfully traversed.

Examiner has stated in the office action that Sugai and Ciciora lack disclosing a control and status register in communication with the comparator command register and the comparator. The invention as recited in claims 2, 4 and 6 requires "a control and status register in communication with the comparator command register and the comparator wherein the control and status register is configured to receive information from the comparator and to send information to the comparator command register and is operable to receive information from a jumper for enabling writing to the mass storage device." Browne does not describe a comparator, a comparator command register or a jumper and how they are connected. Further, details of the circuits used in Browne are not provided. Thus, Browne can't be said to overcome the deficiencies recited in regards to Sugai and Ciciora by the Examiner. Therefore, for at least these reason, the combination Sugai, Ciciora and Browne can't be said to render obvious claim 2, 4 and 6 and the rejection is believed overcome thereby.

The Examiner rejected claims 7, 9 and 11 under U.S.C. 103 (a) as being unpatentable over Sugai (5,564,036) in view of Ciciora (4,091, 418) and in further view of Brunner, et al. (4,727,544). The rejection is respectfully traversed.

The Sugai and Ciciora patents have been distinguished above. The Brunner patent describes a method of software computation of a checksum to ensure the integrity of data stored in EPROMs. Brunner also specifies a method of software computation to ensure that the data stored in these local memories is valid. It does not disclose or suggest a system for protecting its EPROM from write operations.

In gaming machines, as described by Brunner, the EPROM are protected from writes because, by design, EPROMs do not allow writes. Thus, the gaming machine in Brunner does

not provide any mechanisms for writing to an EPROM. This differs from differs from the RAM of Sugai that is normally written to in the course of operating the device in Sugai. On gaming machines, such as those described in Brunner, game programs are updated by physically replacing the EPROM with a new EPROM. The system of Brunner is for confirming that an authorized EPROM has not been installed in the gaming machine not for protecting the EPROM from writes. Thus, because Brunner does not overcome the deficiencies described in regards to Sugai and Ciciora and because Brunner does not teach or suggest a system for protecting memory from writes, the combination of Sugai, Ciciora and Brunner can't be said to render obvious claims 7, 9 and 11 and the rejection is believed overcome thereby.

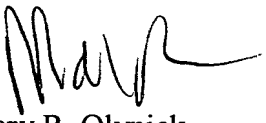
The Examiner rejected claims 8, 10 and 12-14 under U.S.C. 103 (a) as being unpatentable over Sugai (5,564,036) in view of Ciciora (4,091, 418) and in further view of Brunner, et al. (4,727,544) in further view of Browne (6,272,533). The rejection is respectfully traversed.

As described above, the combination Sugai, Ciciora and Browne does not provided, as recite, "a control and status register in communication with the comparator command register and the comparator wherein the control and status register is configured to receive information from the comparator and to be accessible to the comparator command register and is operable to receive information from a jumper for enabling writing to the mass storage device." A control and status register is not taught or suggest in Sugai and Ciciora. Browne or Brunner does not describe a control and status register configured to receive information from the comparator and to send information to the comparator command register and operable to receive information from a jumper for enabling writing to the mass storage device. Therefore, for at least these reasons, the combination of Sugai, Ciciora, Browne and Brunner can't be said to render obvious claims 8, 10 and 12-14 and the rejection is believed overcome thereby.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a

telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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